

EAST SEARCH

11/9/05

L#	Hits	Search String	Databases
S1	32571	(microprocessor\$1 or microcomputer\$1 or computer\$1) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S2	1452	S1 and (performance near2 simulat\$3)	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S3	382	S1 and (functional near2 simulat\$3)	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S4	34	S1 and (cycle near2 accurate near2 simulat\$3)	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S5	73	S2 and S3	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S6	106	S4 or S5	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S7	2	S3 and S4	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S8	106	S6 or S7	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S10	43	S8 and (code with (portion\$1 or part\$1 or section\$1))	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S11	88	S8 and (simulat\$3 with mode\$1)	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S12	44	S8 and ((modif\$4 or chang\$3 or switch\$3) with mode\$1)	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S13	93	S8 and ((simulat\$3 with accuracy) or (code with (portion\$1 or part\$1 or section\$1)) or (simulat\$3 with part\$1 or section\$1))	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S14	1	20030105620 and (simulat\$3 with code with (portion\$1 or part\$1 or section\$1))	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S15	1	20030105620 and (cycle-based same event-based)	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S16	1	6.687662, pn. and ("functional model" same "cycle accurate model")	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S17	32606	(microprocessor\$1 or microcomputer\$1 or computer\$1) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S18	1454	S17 and (performance near2 simulat\$3)	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S19	382	S17 and (functional near2 simulat\$3)	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S22	106	S20 or S21	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S23	2	S19 and S20	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S24	106	S22 or S23	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S25	31	S24 and (simulat\$3 with accuracy)	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S26	3	S24 and ((functional near2 (simulat\$3 or model\$1) with ((delay or execution) near2 time))	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S27	1	S17 and ((functional near2 (simulat\$3 or model\$1) same ((predict\$3 or forecast\$3 or estimat\$3 or model\$1) with ((delay or execution) near2 time)))	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S28	10	S17 and ((functional near2 (simulat\$3 or model\$1) with ((delay or execution) near2 time)))	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S21	73	S18 and S19	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S20	34	S17 and (cycle near2 accurate near2 simulat\$3)	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S31	38	S29 and S30	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S32	1	S29 and "VaST Systems Technology"	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S30	60	S18 and (accuracy with (portion\$1 or part\$1 or section\$1))	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB
S29	492	S18 and ((code or model) with (portion\$1 or part\$1 or section\$1))	US-PGPUB; USPAT; EPO; JPO; DERVENT; IBM_TDB

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Results of search set S23:

Document Kind	Codes Title	Abstract	Issue Date	Current OR
US	20050228628 A1	System-level simulation of interconnected devices	2005/10/13	703/13
US	20050228627 A1	System-level simulation of devices having diverse timing	2005/10/13	703/13
US	20050216702 A1	Dual-processor complex domain floating-point DSP system on chip	2005/09/29	712/35
US	20050193280 A1	Design instrumentation circuitry	2005/09/01	714/47
US	20050192785 A1	Computer simulator for continuously variable transmissions	2005/09/01	703/18
US	20050149313 A1	Method and system for selective compilation of instrumentation entities into a simulation model	2005/07/07	703/22
US	20050138586 A1	Method for verification of gate level netlists using colored bits	2005/06/23	716/5
US	20050125757 A1	Derivation of circuit block constraints	2005/06/09	716/7
US	20050125754 A1	Hardware debugging in a hardware description language	2005/06/09	716/5
US	20050091025 A1	Methods and systems for improved integrated circuit functional simulation	2005/04/28	703/16
US	20050071145 A1	Simulation apparatus, simulation program, and recording medium	2005/03/31	703/19
US	20050071144 A1	Method for providing VHDL model of embedded memory with delay back annotation	2005/03/31	703/19
US	20050055575 A1	Generation of software objects from a hardware description	2005/03/10	717/135
US	20050010880 A1	Method and user interface for debugging an electronic system	2005/01/13	716/4
US	20050010387 A1	High level synthesis device, method for generating a model for verifying hardware, method for using multiple simulation environments	2005/01/13	703/14
US	20040236562 A1	Using multiple simulation environments	2004/11/25	703/22
US	20040236560 A1	Power estimation using functional verification	2004/11/25	703/18
US	20040236559 A1	Statistical approach for power estimation	2004/11/25	703/18
US	20040215438 A1	Hardware and software co-simulation using estimated adjustable timing annotations	2004/10/28	703/22
US	20040210431 A1	Method and apparatus for accelerated post-silicon testing and random number generation	2004/10/21	703/17
US	20040198372 A1	System, method, and computer program product for configuring stochastic simulation models	2004/01/07	703/22
US	20040199366 A1	Mixed signal analog connectivity check system	2004/01/07	703/4
US	20040193395 A1	Program analyzer for a cycle accurate simulator	2004/09/30	703/22
US	20040139411 A1	Heterogeneous design process and apparatus for systems employing static design components	2004/07/15	716/7
US	20040122644 A1	Optimized execution of software objects generated from a hardware description	2004/06/24	703/16
US	20040117168 A1	Global analysis of software objects generated from a hardware description	2004/06/17	703/14
US	20040117167 A1	Simulation of software objects generated from a hardware description	2004/06/17	703/14
US	20040111708 A1	Method and apparatus for identifying similar regions of a program's execution	2004/06/10	717/131
US	20040093197 A1	Mechanism to synchronize probes during simulation of system-level designs	2004/05/13	703/13
US	20040025122 A1	Hardware-based HDL code coverage and design analysis	2004/02/05	716/4
US	20030229482 A1	Apparatus and method for managing integrated circuit designs	2003/12/11	703/14
US	20030182642 A1	Hardware debugging in a hardware description language	2003/09/25	716/4
US	20030177018 A1	System for designing virtual prototypes	2003/09/18	705/1
US	20030162159 A1	Modular computer-based training system	2003/08/28	434/362
US	20030131325 A1	Method and user interface for debugging an electronic system	2003/07/10	716/4
US	20030110920 A1	Power modeling methodology for a pipelined processor	2003/06/12	703/18
US	20030105620 A1	System, method and article of manufacture for interface constructs in a programming language	2003/06/05	703/22
US	20030105617 A1	Hardware acceleration system for logic simulation	2003/06/05	703/14

US 20030074177 A1	System, method and article of manufacture for a simulator plug-in for co-simulation purposes	20030417 703/22
US 20030069724 A1	Method and system for debugging an electronic system using instrumentation circuitry and a local programming language	20030410 703/16
US 20030046671 A1	System, method and article of manufacture for signal constructs in a programming language	20030306 7/17/141
US 20030046668 A1	System, method and article of manufacture for distributing IP cores	20030306 7/17/131
US 20030037321 A1	System, method and article of manufacture for extensions in a programming language capable of supporting multiple cores	20030220 7/17/149
US 20030033594 A1	System, method and article of manufacture for parameterized expression libraries	20030213 7/17/141
US 20030033588 A1	System, method and article of manufacture for using a library map to create and maintain IP cores	20030213 7/17/107
US 20030028864 A1	System, method and article of manufacture for successive compilations using incomplete parallel processing	20030206 7/17/141
US 20030023533 A1	Multidimensional method and system of simulating and managing an "Alliance Investment Portfolio"	20030130 705/36
US 20030009746 A1	Variable accuracy modes in microprocessor simulation	20030109 7/17/135
US 20030005090 A1	System and method for integrating network services	20030102 709/220
US 20020199173 A1	System, method and article of manufacture for a debugger capable of operating across multiple IP cores	20021226 7/17/129
US 20020172203 A1	Fast IP route lookup with 16/K and 16/Kc compressed data structures	20021121 370/392
US 20020144212 A1	System, method and computer program product for web-based integrated circuit design	20021003 716/1
US 20020133325 A1	Discrete event simulator	20020919 703/17
US 20020128809 A1	Randomized simulation model instrumentation	20020905 703/17
US 20020123874 A1	Detecting events within simulation models	20020905 703/17
US 20020123873 A1	Signal override for simulation models	20020829 717/143
US 20020120922 A1	Embedded hardware description language instrumentation	20020808 703/14
US 20020107678 A1	Virtual computer verification platform	20020103 716/4
US 20020002698 A1	Method for verifying the design of a microprocessor	20011025 703/14
US 20010034594 A1	Design verification method, design verification device for microprocessors, and pipeline simulation circuitry	20050816 714/34
US 6931572 B1	Detecting events within simulation models	20050719 703/17
US 6920418 B2	Hardware debugging in a hardware description language	20050607 716/4
US 6904577 B2	Power modeling methodology for a pipelined processor	20050517 716/1
US 6895561 B2	Endoscopic tutorial system with a bleeding complication	20050308 434/272
US 6863536 B1	Method and user interface for debugging an electronic system	20041123 716/4
US 6823497 B2	Method and apparatus for modeling using a hardware-software co-verification environment	20041026 703/14
US 6810373 B1	Retargetable computer design system	20040803 703/21
US 6772106 B1	System, method and computer program product for web-based integrated circuit design	20040525 716/1
US 6742165 B2	Method and apparatus for producing modules compatible with a target system platform from simulation	20040316 717/136
US 6708329 B1	System, method and article of manufacture for signal constructs in a programming language capable of supporting multiple cores	20040210 717/114
US 6691301 B2	System and method for automated design verification	20040203 703/14
US 6678645 B1	Method and apparatus for SoC design validation	20040113 703/20
US 6625572 B1	Cycle modeling in cycle accurate software simulators of hardware modules for software/software verification	20030923 703/19
US 6618839 B1	Method and system for providing an electronic system design with enhanced debugging capabilities	20030909 716/4
US 6581191 B1	Hardware debugging in a hardware description language	20030617 716/4
US 6523151 B2	Method for verifying the design of a microprocessor	20030218 716/4
US 6513126 B1	SYSTEM FOR MODELING A PROCESSOR-ENCODER INTERFACE BY COUNTING NUMBER OF CYCLES	20030128 713/500
US 6507809 B1	Method and system for simulating performance of a computer system	20030114 703/21
US 6487704 B1	System and method for identifying finite state machines and verifying circuit designs	20021126 716/5
US 6470478 B1	Method and system for counting events within a simulation model	20021022 716/4

US 6466898 B1	Multithreaded, mixed hardware description languages logic simulation on engineering workstations	20021015 703117
US 6389379 B1	Conversion system and method	20020514 703114
US 6370494 B1	Simulator and computer-readable recordable medium having program for execution on computer	20020409 703117
US 6321295 B1	System and method for selective transfer of application data between storage devices of a computer	20011120 711/117
US 6223142 B1	Method and system for incrementally compiling instrumentation into a simulation model	20010424 703115
US 6212491 B1	Automatic adjustment for counting instrumentation	20010403 703114
US 6202042 B1	Hardware simulator instrumentation	20010313 703116
US 6195629 B1	Method and system for selectively disabling simulation model instrumentation	20010227 703117
US 6195627 B1	Method and system for instrumenting simulation models	20010227 703114
US 6192504 B1	Methods and systems for functionally describing a digital hardware design and for converting a	20010220 716/1
US 6161211 A	Method and apparatus for automated circuit design	20001212 716/1
US 6141630 A	System and method for automated design verification	20001031 703114
US 6110223 A	Graphic editor for block diagram level design of circuits	20000829 716/18
US 6097885 A	Digital system simulation	20000801 703117
US 6087967 A	Method for generating and reading a compressed all event trace file	20000711 341/63
US 6052524 A	System and method for simulation of integrated hardware and software components	20000418 703122
US 6047387 A	Simulation system for testing and displaying integrated circuit's data transmission function of p	20000404 714/33
US 6028996 A	Method and apparatus for virtualizing system operation	20000222 703128
US 5966537 A	Method and apparatus for dynamically optimizing an executable computer program using input	19991012 717/158
US 5838948 A	System and method for simulation of computer systems combining hardware and software integr	19981117 703127
US 5815687 A	Apparatus and method for simulating domino logic circuits using a special machine cycle to vali	19980929 703114
US 5801958 A	Method and system for creating and validating low level description of electronic design from hi	19980901 716/18
US 5752002 A	Method and apparatus for performance optimization of integrated circuit designs	19980512 703114
US 5752000 A	System and method for simulating discrete functions using ordered decision arrays	19980512 703114
US 5727187 A	Method of using logical names in post-synthesis electronic design automation systems	19980310 716/18
US 5717699 A	Method and apparatus for accessing internal integrated circuit signals	19980210 714/725
US 5680590 A	Simulation system and method of using same	19971021 70312
US 5678028 A	Hardware-software debugger using simulation speed enhancing techniques including skipping, i	19971014 703122
US 5675757 A	Direct match data flow memory for data driven computing	19971007 712/201
US 5657465 A	Direct match data flow machine apparatus and process for data driven computing	19970812 712/201
US 5650938 A	Method and apparatus for verifying asynchronous circuits using static timing analysis and dynal	19970722 716/6
US 5623418 A	System and method for creating and validating structural description of electronic system	19970422 716/1
US 5615357 A	System and method for verifying processor performance	19970325 703121
US 5555201 A	Method and system for creating and validating low level description of electronic design from hi	19960910 716/1
US 552984 A	Diagnostic system for complex systems using virtual components	19960903 701/31
US 550762 A	Diagnostic system for electronic automotive system	19960827 702/183
US 546562 A	Method and apparatus to emulate VLSI circuits within a logic simulator	19960813 703114
US 544067 A	Method and system for creating, deriving and validating structural description of electronic syst	19960806 703114
US 5465368 A	Data flow machine for data driven computing	19951107 712/27
US 5394346 A	Simulation of an electronic system including analog and digital circuitry using high level macro	199505228 703114
US 5392227 A	System and method for generating electronic circuit simulation models having improved accuracy	19950221 703114
US 5313615 A	Block diagram simulator using a library for generation of a computer program	19940517 716/11
US 5263149 A	Integrated circuit logic functions simulator for selectively connected series of preprogrammed F	19931116 703115

US 5151984 A	Block diagram simulator using a library for generation of a computer program	19920929 703122
US 5146460 A	Logic simulation using a hardware accelerator together with an automated error event isolation	19920908 714133
US 5111413 A	Computer-aided engineering	19920505 703114
US 4870561 A	User interface simulation and management for program-controlled apparatus	19890926 700187
US 4787061 A	Dual delay mode pipelined logic simulator	19881122 703114
US 4763288 A	System for simulating electronic digital circuits	19880809 703119
US 4744084 A	Hardware modeling system and method for simulating portions of electrical circuits	19880510 714133
US 4621524 A	Circuit layout for the simulation of moments of inertia on test stands	19861111 731116
US 3996457 A	Electronic analog computers	19761207 7081800
US 200500555675 A	Software object generation method for simulating electronic hardware device, involves using gl	20050310
US 200401933395 A	Program analyzing during microprocessor development, involves executing program on processor	20040930
US 20040117168 A	Software object analysis method in electronic device simulation, involves reducing coded description	20040617
US 20030009746 A	Performance simulation method for computer system, involves applying functional and performance	20030109
US 6167363 A	Comparison of model simulation output signal of logic circuit, involves starting RTL and HDL model	20011226